REMARKS

Claims 1-7, 14-18, and 28-31 are all the claims presently pending in the application. Claims 1, 14-15 and 17 have been amended to more clearly define the invention and claims 28-31 have been added. Claims 1, 14-15 and 17 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Support for these amendments may be found in the specification at, for example, page 5, lines 15-16 and page 6, lines 2-3. Therefore, no new matter is introduced by these amendments.

Applicants also note that, notwithstanding any claim amendments herein or later during prosecution, Applicants intent is to encompass equivalents of all claim elements.

Claims 1-7, 11 and 14-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nishizawa, et al. (U.S. Patent No. 4,939,571). Claims 1- 2, 6 and 14-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Ma, et al. (U.S. Patent No. 6,407,435 B1). Claims 1, 4 and 15-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamazaki (U.S. Patent No. 5,094,966). Claims 1-4, 7, and 14-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Goldman, et al. (U.S. Patent No. 4,151,537).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a field effect transistor that includes a substrate, an insulating layer and a gate electrode. The substrate includes a source region, a drain region, and a channel. The insulating layer is disposed over the channel region and includes an insulating layer having an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer disposed over the channel region. The gate electrode is disposed over the insulating layer and the aluminum nitride layer has a thickness that is within a range of about 0.1 nm to about 10 nm.

Conventional high dielectric constant gate dielectrics for silicon complementary metal oxide semiconductor (CMOS) devices, such as transistors, use a silicon dioxide gate dielectric or silicon oxynitride. As CMOS devices miniaturize, scaling laws require that the ratio of permittivity and thickness of the dielectric layer also reduce.

However, when the layer is below a thickness of 1.5 - 1.7 nanometers, the layer starts transmitting an unacceptably high amount of leakage current. Additionally, as the layer gets so thin, it also becomes impervious to the diffusion of impurities, or dopant atoms. Therefore, the dielectric layer fails to protect the underlying silicon substrate.

By contrast, the present invention includes an insulating layer that has an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer. In this manner, the present invention provides a high dielectric constant gate dielectric for a CMOS transistor. In comparison with silicon dioxide, whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of

approximately 9 - 16.

As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

Further, regarding the thicknesses of the layers recited by claims 1, 14-15, 17, and 28-31, as explained above, the conventional devices have been unable to reduce the thickness of the gate dielectric stack to satisfy scaling laws regarding the relationship between permittivity and thickness because anything below a thickness of 1.5 - 1.7 nanometers have resulted in an unacceptably high amount of leakage current and these layers fail to protect the underlying silicon substrate below the dielectric layer from the diffusion of impurities, or dopant atoms.

In stark contrast, an exemplary embodiment of the present invention provides a thin gate dielectric that solves the above-described problems. A first exemplary embodiment of the invention provides an aluminum nitride layer that is as thin as about 0.1 nm to about 10 nm and a second exemplary embodiment provides an aluminum oxide layer taht is about 0.1 nm to about 2.0 nm.

II. THE PRIOR ART REJECTIONS

A. The Nishizawa et al. reference

Regarding the rejection of claims 1-7, 11 and 14-18, the Examiner alleges that the Nishizawa et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by these references.

Contrary to the allegations of the Examiner, the Nishizawa et al. reference does not teach or suggest the features of independent claims 1, 14-15 and 17 including an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer. This feature is important for providing a high dielectric constant gate dielectric for a CMOS transistor.

In comparison with silicon dioxide, whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

Rather, the Nishizawa et al. reference discloses an insulated-gate type transistor. In particular, the Nishizawa et al. reference discloses an insulating layer 6 with silicon dioxide, aluminum oxide, silicon nitride or aluminum nitride (Fig. 1, col. 2, lines 9-10; and col. 3, lines 37 - 39). Thus, the Nishizawa et al. reference merely discloses that an insulating layer may be made out of any combination of silicon dioxide, aluminum oxide, silicon nitride or aluminum nitride.

Indeed, the Examiner appears to recognize that fact by asserting that "this phrase covers every combination of the four dielectric layers." However, the claims of the present application do not recite "every combination of the four dielectric layers."

To the contrary, the claims of the present application recite an insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer. In other words, while the Nishizawa et al. reference appears to disclose a very broad combination of materials, the claims of the present invention recite a specific subset of that combination which provides specific advantages.

It is the specific subset which the claims recite and which are not disclosed by the Nishizawa et al. reference and which enables the present invention to provide the advantages discussed above, and which the Examiner agrees is not disclosed by the Nishizawa et al. reference.

As agreed by the Examiner, the Nishizawa et al. reference does not provide the benefits that the aluminum nitride layer in combination with at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has over conventional silicon dioxide and an aluminum nitride layer alone.

As evidenced by the listing in the Nishizawa et al. reference at col. 2, lines 9-10, appears to disclose that silicon dioxide and aluminum nitride are interchangeable. The present invention specifically recites an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer. It is this feature which provides the advantages of the invention. Clearly, the Nishizawa et al. reference does not teach or suggest this feature and, as a result, the features disclosed by the Nishizawa et al. reference are incapable of providing the advantages of the present invention.

As explained above, the aluminum nitride in combination with at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer is important because it provides a high dielectric constant gate dielectric for a CMOS transistor. In comparison with Silicon dioxide whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

The Nishizawa et al. reference does not teach or suggest features of the independent claims including an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer.

Further, the Nishizawa et al. reference also does not teach or suggest the features of the independent claims including an aluminum nitride layer that has a thickness that is within a range of about 0.1 nm to about 10 nm. Indeed, the Nishizawa et al. reference does not teach or suggest anything at all regarding thicknesses.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1-7, 11 and 14-18.

B. The Ma et al. reference

Regarding the rejection of claims 1-2, 6 and 14-18, the Examiner alleges that the Ma et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by these references.

Contrary to the allegations of the Examiner, the Ma et al. reference does not teach or suggest the features of independent claims 1, 14-15 and 17 including an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer.

This feature is important for providing a high dielectric constant gate dielectric for a CMOS transistor. In comparison with silicon dioxide, whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet

still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

Rather, the Ma et al. reference discloses a multilayer dielectric stack and method of producing that stack. The Ma et al. reference discloses a multilayer dielectric stack 116 which includes an interposing layer 130 between a high dielectric layer 140 and the silicon substrate 112 (Fig. 2).

In a manner similar to the Nishizawa et al. reference, the Ma et al. reference discloses that the interposing layer 130 may include aluminum oxide, aluminum nitride, silicon nitride or silicon dioxide (col. 1, lines 64-67). Thus, the Ma et al. reference merely discloses that an insulating layer may be made out of any combination of silicon dioxide, aluminum oxide, silicon nitride or aluminum nitride.

Indeed, the Examiner appears to recognize that fact by asserting that "this phrase covers every combination of the four dielectric layers." However, the claims of the present application do not recite "every combination of the four dielectric layers".

To the contrary, the claims of the present application recite an insulating layer which

includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer. In other words, while the Ma et al. reference appears to disclose a very broad combination of materials, the claims of the present invention recite a specific subset of that combination which provides specific advantages.

It is the specific subset which the claims recite and which are not disclosed by the Ma et al. reference and which enables the present invention to provide the advantages discussed above, and which the Examiner agrees is not disclosed by the Ma et al. reference.

Additionally, the Ma et al. reference does not disclose the benefits that the aluminum nitride layer in combination with at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has over conventional silicon dioxide and an aluminum nitride layer alone.

As evidenced by the listing in the Ma et al. reference at col. 1, lines 64-67, appears to disclose that silicon dioxide and aluminum nitride are interchangeable. Clearly, the Ma et al. reference does not provide the advantages of the present invention.

As explained above, the aluminum nitride in combination with at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer is important because it provides a high dielectric constant gate dielectric for a CMOS transistor. In comparison with silicon dioxide whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer

will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

The Ma et al. reference does not teach or suggest features of the independent claims including an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer.

Further, the Ma et al. reference also does not teach or suggest the features of the independent claims including an aluminum nitride layer that has a thickness that is within a range of about 0.1 nm to about 10 nm.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1-2, 6 and 14-18.

C. The Yamazaki reference

Regarding the rejection of claims 1, 4 and 15-18, the Examiner alleges that the Yamazaki reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by these references.

Contrary to the allegations of the Examiner, the Yamazaki reference does not teach or

suggest the features of independent claims 1, 14-15 and 17 including an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer.

This feature is important for providing a high dielectric constant gate dielectric for a CMOS transistor. In comparison with silicon dioxide, whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

Rather, the Yamazaki reference discloses forming a gate insulating layer 5 including a silicon oxide layer 5a formed on the substrate and a second insulating silicon or aluminum nitride 5b formed on the silicon oxide layer 5a (col. 4, lines 46-50).

Therefore, contrary to the Examiner, the Yamazaki reference does not teach or suggest an insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer. In other words, while the Yamazaki reference appears to disclose a silicon oxide layer, the Yamazaki reference does not disclose a

silicon dioxide, an aluminum oxide or a silicon nitride layer.

Further, the Yamazaki reference also does not teach or suggest the features of the independent claims including an aluminum nitride layer that has a thickness that is within a range of about 0.1 nm to about 10 nm.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1, 4 and 15-18.

D. The Goldman et al. reference

Regarding the rejection of claims 1-4, 7, and 14-18, the Examiner alleges that the Goldman et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by these references.

Contrary to the allegations of the Examiner, the Goldman et al. reference does not teach or suggest the features of independent claims 1, 14-15 and 17 including an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer.

This feature is important for providing a high dielectric constant gate dielectric for a CMOS transistor. In comparison with silicon dioxide, whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon

dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

Rather, the Goldman et al. reference discloses insulating layers of silicon nitride 22, silicon oxy-nitride 24 and silicon dioxide 26 and that other materials such as aluminum oxide and aluminum nitride may be substituted for any of these layers (col. 2, lines 65-68).

Therefore, in a manner similar to the Nishizawa et al. reference and the Ma et al. reference, the Goldman et al. discloses that the insulating layers may be made out of any combination of silicon nitride, silicon oxy-nitride, silicon dioxide, aluminum oxide and aluminum nitride.

To the contrary, the claims of the present application recite an insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer. In other words, while the Goldman et al. reference appears to disclose a very broad combination of materials, the claims of the present invention recite a specific subset of that combination which provides specific advantages.

It is the specific subset which the claims recite and which are not disclosed by the Goldman et al. reference and which enables the present invention to provide the advantages discussed above, and which the Examiner agrees is not disclosed by the Goldman et al. reference.

Additionally, the Goldman et al. reference does not recognize the benefits that the aluminum nitride layer in combination with at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has over conventional silicon dioxide and an aluminum nitride layer alone.

As evidenced by the listing in the Goldman et al. reference at col. 2, lines 65-68, appears to disclose that silicon dioxide and aluminum nitride are interchangeable. Clearly, the Goldman et al. reference does not teach or suggest the advantages of the present invention.

As explained above, the aluminum nitride layer in combination with at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer is important because it provides a high dielectric constant gate dielectric for a CMOS transistor. In comparison with silicon dioxide whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

Moreover, as explained in detail in the specification at, for example, page 6, line 20 - page 7, line 11, the insulating layer which includes an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer has advantages over the conventional silicon dioxide layer and an aluminum nitride layer alone.

The Goldman et al. reference does not teach or suggest features of the independent claims including an aluminum nitride layer and at least one of an aluminum oxide layer, a silicon dioxide layer, and a silicon nitride layer.

Further, the Goldman et al. reference also does not teach or suggest the features of the independent claims including an aluminum nitride layer that has a thickness that is within a range of about 0.1 nm to about 10 nm.

Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1-4, 7, and 14-18.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that claims 1-7, 14-18, and 28-31, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 11/17/03

James E. Howard
Registration No. 39,715

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that I am filing this Supplemental Amendment and Petition and Fee for One-Month Extension of Time by facsimile with the United States Patent and Trademark Office to Examiner Kevin V. Quinto, Group Art Unit 2826 at fax number (703) 872-9319 this 17th day of November, 2003.

James E. Howard
Reg. No. 39,715